Amendments to the Claims:

1. (currently amended) An apparatus for converting a source frame signal to a destination frame signal, wherein the source frame signal is received at a first frame rate and the destination frame signal is output at a second frame rate, comprising:

a converter for converting the source frame signal to the destination frame signal having a destination clock signal at a destination clock frequency; and

a frequency synthesizer for generating the destination clock signal and dynamically adjusting the destination clock frequency such that the first frame rate and the second frame rate are substantially the same~~.~~;

wherein the destination display signal includes a last horizontal line defined by a last horizontal sync signal and a vertical sync signal, wherein the last horizontal sync signal is the last of a plurality of horizontal sync signals, and the frequency synthesizer synchronously generates the output vertical sync signal with the horizontal sync signal during the last horizontal line.

2. (original) The apparatus of claim 1 wherein the source frame signal is at a first resolution and the destination frame signal is at a second resolution.

3. (original) The apparatus of claim 1 further comprising:

a buffer for storing at least a part of the source frame signal;

wherein the frequency synthesizer adjusts the destination clock frequency by decreasing the destination clock frequency to prevent underflow in the buffer or by

increasing the destination clock frequency to prevent overflow in the buffer.

4. (original) The apparatus of claim 1 wherein the frequency synthesizer adjusts the destination clock frequency by decreasing the destination clock frequency when the second frame rate is faster than the first frame rate or by increasing the destination clock frequency when the second frame rate is slower than the first frame rate.

5. (cancelled)

6. (original) The apparatus of claim 1 wherein the converter receives the source frame signal at a source clock signal, and the destination clock signal is independent on the source clock signal.

7. (original) The apparatus of claim 1 wherein the frequency synthesizer is a phase-locked loop (PLL).

8. (original) The apparatus of claim 1 wherein the converter is a scaler.

9. (currently amended) A method of frame synchronization for converting a source frame signal to a destination frame signal, wherein the source frame signal is received at a first frame rate, the destination frame signal is output at a second frame rate, comprising:

generating the destination frame signal according to the source frame signal, wherein the destination frame signal includes a destination clock signal at a destination clock frequency; and

dynamically adjusting the destination clock frequency such that the first frame rate

and the second frame rate are substantially the same.;

wherein the destination frame includes a last horizontal line defined by a last horizontal sync signal and a vertical sync signal, wherein the last horizontal sync signal is the last of a plurality of horizontal sync signals, the method further comprising the step of synchronously generating the output vertical sync signal with the horizontal sync signal during the last horizontal line.

10. (original) The method of claim 9 wherein the source frame signal is at a first resolution and the destination frame signal is at a second resolution.

11. (original) The method of claim 9 wherein the step of adjusting the destination clock frequency is executed by decreasing the destination clock frequency to prevent underflow or by increasing the destination clock frequency to prevent overflow.

12. (original) The method of claim 9 wherein the step of adjusting the destination clock frequency is executed by decreasing the destination clock frequency when the second frame rate is faster than the first frame rate or by increasing the destination clock frequency when the second frame rate is slower than the first frame rate.

13. (cancelled)

14. (original) The method of claim 9 wherein the destination clock frequency has a first resolution such that the first frame rate and the second frame rate are substantially the same.

15. (currently amended) The method of claim 14 wherein the destination clock frequency is adjusted utilizing an adjustment resolution being ~~first resolution is~~

approximately satisfied by ~~A first resolution <~~ $\frac{1}{2} \frac{(HorizontalVisible)}{HorizontalTotal \bullet VerticalTotal}$,

~~wherein the~~

Adjustment resolution < $\frac{1}{2} \frac{(HorizontalVisible)}{HorizontalTotal \bullet VerticalTotal}$, wherein the *HorizontalVisible* parameter refers to the number of visible pixels in each horizontal line, the *HorizontalTotal* parameter refers to the total number of pixel data for each horizontal line, the *VerticalTotal* parameter refers to the total number of horizontal lines in each frame.

16. (currently amended) A method of frame synchronization for converting a source frame signal to a destination frame signal, wherein the source frame signal is received at a first frame rate, the destination frame signal is output at a second frame rate, comprising:

generating the destination frame signal according to the source frame signal, wherein the destination frame signal includes a destination clock signal at a destination clock frequency; and

dynamically adjusting a period of the destination frame signal such that the first frame rate and the second frame rate are substantially the same~~.~~;

wherein the destination frame includes a last horizontal line defined by a last horizontal sync signal and a vertical sync signal, the last horizontal sync signal is the last of a plurality of horizontal sync signals, the method further comprising the step of synchronously generating the vertical sync signal according to the horizontal sync signal during the last horizontal line.

17. (cancelled)